What is Claimed is:

1. A delay lock loop for an FPGA architecture comprising:

a reference delay line having an input and an output, said input coupled to reference clock;

a feedback delay line having an input and an output; said input coupled to a feedback clock;

a divide-by-two circuit having an input and an output, said input coupled to said output of said reference delay line;

a phase detector having first input, a second input, and a plurality of outputs, said first input coupled to said output of said divide-by-two circuit, and said second input coupled to said output of said feedback delay line;

a control circuit having a plurality of inputs and a plurality of outputs, said plurality of inputs coupled to said plurality of output of said phase detector;

a programmable delay line having a reference clock input, a plurality of data inputs, and an output, said reference clock input coupled to said reference clock, said plurality of data inputs coupled to said plurality of outputs of said control circuit to receive data to program a delay in said programmable delay line in the operation of the DLL;

a clock doubler having an input and an output, said input coupled to said output of said programmable delay line; and

a clock tree having an input and an output, said input coupled to said output of said clock doubler, and said output forming the feedback clock coupled to said input of said feedback delay line.